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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,503	10/25/2002	William R. Corbin	BUR920010217US1	2123

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INTELLECTUAL PROPERTY LAW
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EXAMINER	
KERVEROS, JAMES C	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,503	CORBIN ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *1-11 and 14* is/are allowed.

6)☒ Claim(s) *12 and 13* is/are rejected.

7)☒ Claim(s) *1-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This is a Non-Final Office Action in response to Amendment filed 9/15/2005, in reply to the prior Office Action dated 6/28/2005.

Claims 1-14 are pending.

Prior Office Action Claim Objections is herby withdrawn in view of the Amendment to the claims.

Prior Office Action Claim Rejections under 35 USC § 112 is herby withdrawn in view of the Amendment to the claims.

Response to Arguments

Applicant's arguments, see Remarks of the Amendment filed 9/15/2005, with respect to claims 1-11 and 14 have been fully considered and are persuasive. The rejection of 1-11 and 14 has been withdrawn. Claims 1-11 and 14 are allowed.

Applicant's arguments filed 9/15/2005 with respect to claims 12 and 13 have been considered but are moot in view of a new ground of rejection, under 35 U.S.C. 103(a) as being unpatentable over Kim (U. S. Patent NO: 6,122,762) in view of Clark (U.S. Patent No: 6,650,589).

Claim Objections

Claims 1-11 are objected to because of the following informalities:

Claim 1, on line 8, the term "and" should be added after the semicolon.

Claims 2-11 are also objected because of their dependency from an objected claim. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (U. S. Patent NO: 6,122,762) in view of Clark (U.S. Patent No: 6,650,589).

Regarding Claim 12, Kim discloses a method using an integrated circuit memory interface device (40 and 80) representing a memory interface chip including a JTAG circuit, and a DRAM device chip, respectively, and further including a debug controller 400 and a TAP (Test Access Port) controller 100, for performing simultaneous tests of core logic 310 and memory device 80, Figures 4 and 5, comprising:

Clocking the logic the core logic 310 and memory device 80 using (Clockdr) to clock logic 310 and (DRAM.sub.-- clk) to cock the memory device 80. The data boundary-scan register 332 captures data from the core logic 310 in synchronism with the clock signal (Clockdr) and the (DRAM.sub.-- clk) operates the DRAM device, and generates a third clock signal (e.g. Din.sub.-- cap.sub.-- clk). The data boundary-scan

register captures data from the core logic in synchronism with the second clock signal (Clockdr) and data from the DRAM device in synchronism with the third clock signal (Din.sub.-- cap.sub.-- clk).

Enabling and disabling the BIST (debug controller 400) scan chain bypass isolation element (multiplexer 340), which selects a bypass register 320 or a boundary scan register 330 surrounding core logic 310 of the interface device chip 40. The bypass register 320 is a single-bit register that is placed between the TDI and the TDO. When selected, the bypass register 320 provides a single-bit scan path between the TDI and the TDO. Thus, the bypass register 320 abbreviates the scan path through devices that are not involved in the test. The bypass register 320 is selected when the instruction register is loaded with a pattern of all ones to satisfy the IEEE Std 1149.1 BYPASS instruction requirement. Testing the memory device 80, while reading out TDO from the boundary scan register 330.

Kim does not explicitly disclose, separating the logic and memory circuits using isolation elements. However, Clark, in analogous art, discloses voltage isolation elements, such as voltage regulator 90 that provides one operating voltage to microprocessor core 20 and a separate operating voltage to memory block 40, (Figure 2, Clark).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate a voltage regulator as taught by Clark in the semiconductor integrated device of Kim, so as maintain isolation between the logic and memory operating voltage, since an integrated circuit having a microprocessor core

and a memory block may operate at different voltages. Therefore, the voltage regulator generates two operating voltages, one for the microprocessor core to satisfy power and performance criteria, and the other operating voltage for the memory block to provide acceptable noise margins and maintain stability of the memory cells within the memory block (Abstract, Clark).

Regarding Claim 13, Kishi discloses testing the bypass isolation elements. When the BYPASS instruction is loaded in the instruction register 210 and the TAP is placed in a Shift.sub.-- DR state, the bypass register 320 is placed between the TDI and the TDO. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Allowable Subject Matter

Claims 1-11 and 14 are allowed.

The prior arts of record taken alone or in combination fail to teach, anticipate, suggest or render obvious the claimed invention, recited in the independent claim 1, including inter alia, a clocking system having clocking isolation elements for logic and memory circuits and scan chain by pass isolation elements to enable and disable the BIST which tests the memory macro circuits while logic scan chain results are read out.

Independent claim 14 recites a method, including inter alia, placing the device into a bypass mode wherein the memory macro circuits are isolated from the scan chains, and generating separate test clock signals to both memory macro circuits and logic circuits.

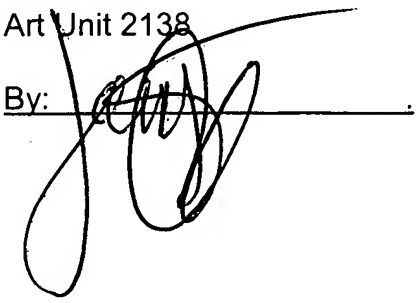
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAMES C KERVEROS
Examiner
Art Unit 2138

By: 

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Date: 3 November 2005
Office Action: Non-Final Rejection